US-PAT-NO: 6175138

DOCUMENT-IDENTIFIER: US 6175138 B1

TITLE: Semiconductor memory device and method of manufacturing the same

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Brief Summary Text - BSTX (18):
This means that new other power supply circuit must be prepared. In consequence, a **peripheral** circuit of the SRAM becomes complex. Further, a circuit for generating the intermediate potential generally increases consumption current (namely, stand-by current) during the stand-by operation.

Brief Summary Text - BSTX (38):
Moreover, the third potential becomes unnecessary by using only the two kinds of potentials, as mentioned above. In consequence, the **peripheral** circuit of the SRAM does not become complex.

Drawing Description Text - DRTX (27):
FIG. 26 is a circuit diagram showing a structure of a **peripheral** circuit of a semiconductor memory device according to the first embodiment of this invention;

Drawing Description Text - DRTX (28):
FIG. 27 is an operational waveform diagram of the **peripheral** circuit illustrated in FIG. 26;

Detailed Description Text - DETX (35):
Surfaces of the gate electrodes 10 and 16 are coated with a first interlayer insulating film 20. Herein, the first **interlayer** insulating film 20 is formed by an oxide film made by the CVD method, a **BSG** (Boron-Silicate Glass) film, a PSG (Phospho-Silicate Glass) film, and a **BPSG** (Boron-Phospho-Silicate Glass) film and the like.

Detailed Description Text - DETX (38):
Surfaces of the W plugs 23a, 23b and the W plugs 24a, 24b is coated with a second interlayer insulating film 26. In this event, the second **interlayer** insulating film is formed by an oxide film made by the CVD method, the **BSG**

film, the PSG film, and the **BPSG** film and the like. In this event, viaholes 27a and 27b are formed in the second interlayer insulating film 26.

Detailed Description Text - DETX (41):

A surface of the first metal wiring line 29a is coated with a third interlayer insulating film 30. In this event, the third **interlayer** insulating film 30 is formed by an oxide film made by the CVD method, the **BSG** film, the PSG film, and the **BPSG** film and the like.

Detailed Description Text - DETX (51):

Further, a **peripheral** circuit is placed around the memory cell consisting of the driving MOS transistors 3, 4 and the MOS transistors 5, 6. In this case, the **peripheral** circuit is composed of N-type MOS transistors and P-type MOS transistors.

Detailed Description Text - DETX (52):

In this **peripheral** circuit, threshold voltage of the N-type and P-type MOS transistors are substantially identical to each other to satisfy a high-speed operation and low stand-by current during the stand-by operation.

Detailed Description Text - DETX (53):

Herein, it is to be noted that the threshold voltage of each driving MOS transistor 3, 4 consisting of the N-type MOS transistor is set larger than that of the N-type MOS transistor in the **peripheral** circuit.

Detailed Description Text - DETX (55):

First, an oxide film 36 is deposited to a film thickness of about 15 nm by the thermal oxidation method on a P-type semiconductor substrate 1, as illustrated in FIG. 7. In this event, a device isolation trench 19 is formed in the semiconductor substrate 1 in advance. Herein, it is to be noted that a memory cell is formed at a right-hand region on the basis of a central portion of the semiconductor substrate 1 while a **peripheral** circuit is formed at a left-hand region on the basis of the central portion.

Detailed Description Text - DETX (56):

Successively, a region for forming a P-type MOS transistor which constitutes each MOS transistors 5, 6 for selecting an address in the memory cell and a region for forming a P-type MOS transistor in the **peripheral** circuit are masked by a photoresist film 37.

Detailed Description Text - DETX (78):

Likewise, the N-type MOS transistor 45 and the P-type MOS transistor 46 are

formed in the **peripheral** circuit.

Detailed Description Text - DETX (79):
Subsequently, an opening portion is formed on a surface of the P.sup.+ -type region 13b of the P-type source region 13, as shown in FIG. 17. Thereafter, a first interlayer insulating film 20 is deposited on the entire surface. Herein, the first **interlayer** insulating film 20 is formed by the oxide film made by the CVD method, the **BSG** film, the PSG film, and the **BPSG** film.

Detailed Description Text - DETX (95):
Next, a second interlayer insulating film 26 is deposited on an entire surface, as illustrated in FIG. 21. Herein, it is to be noted that the second **interlayer** insulating film 26 is formed by the oxide film made by the CVD method, the **BSG** film, the PSG film, and the **BPSG** film. Thereafter, viaholes 27a, 27b are formed by the use of the photolithography method. Successively, W is buried in each viahole 27a, 27b by the CVD method to form each W plug 28a, 28b.

Detailed Description Text - DETX (98):
Next, a third interlayer insulating film 30 is formed on an entire surface by the CVD method, as illustrated in FIG. 23. Herein, it is to be noted that the third **interlayer** insulating film 30 is formed by the oxide film made by the CVD method, the **BSG** film, the PSG film, and the **BPSG** film. Thereafter, a viahole 31 is

Detailed Description Text - DETX (110):
In the meanwhile, a **logic** product (for example, having the gate length of 0.25 .mu.m or less) is increasingly miniaturized in future. In such a **logic** product, the **peripheral** circuit tends to have relatively low threshold voltage (for example, 0.4V or less).

Detailed Description Text - DETX (112):
The **peripheral** circuit illustrated in FIG. 26 includes a writing portion 47, a memory cell 70, a bit line pre-charge portion 48, and a sense amplifier 49. In this event, the writing portion 47 writes a data signal into the memory cell 70. The bit line pre-charge portion 48 supplies the power supply potential to the bit line when all of memory cells connected to the bit line are in a non-selective state.

Detailed Description Text - DETX (116):
The sense amplifier 49 is, for example, is structured by an amplifier circuit, such as, the current/mirror type amplifier. Further, each of

transistors which constitute the **peripheral** circuit has the same threshold voltage mentioned before. Moreover, the power supply voltage is set to 2.5 V.

Detailed Description Text - DETX (117):
Subsequently, description will be made about an operation of the **peripheral** circuit with reference to operation waveform illustrated in FIG. 27.

Detailed Description Text - DETX (138):
Moreover, the third potential becomes unnecessary by using only the two kinds of potentials, as mentioned above. In consequence, the **peripheral** circuit of the SRAM does not become complex.

Detailed Description Text - DETX (149):
In this event, the surface of the local wiring line 25 is coated with the second **interlayer** insulating film 26 which is formed by an oxide film formed by the CVD method, a **BSG** film, a PSG film, and a **BPSG** film.

Claims Text - CLTX (38):
a **peripheral** circuit which has a fifth MIS transistor and a sixth MIS transistor,

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See image for Certificate of Correction

TITLE: MATRIX SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE USING THE SAME IN WHICH THE DISTANCE BETWEEN THE UPPER SURFACE OF THE PIXELS BEING LESS THAN THE DISTANCE BETWEEN THE LOWER SURFACE OF THE PIXELS IN CONTACT WITH THE SUBSTRATE

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Brief Summary Text - BSTX (10):
The method for making an active matrix substrate for the reflection-type liquid crystal display device disclosed in Japanese Patent Laid-Open No. 9-73103 will now be described with reference to FIG. 32. Although FIG. 32 shows a pixel region, peripheral driving circuits such as shift registers for driving **switching transistors** in the pixel region can also be formed on the same substrate.

Brief Summary Text - BSTX (17):
The reflection-type liquid crystal device is driven as follows. Peripheral circuits including a shift register which is formed on the substrate 201 by an on-chip process applies a signal potential to the source region 207 and a gate potential to the gate electrode 205 such that the **switching transistor** in the pixel in an ON state supplies signal charge to the drain region 207'. The signal charge is accumulated in a pn-junction cavity capacitor formed between the drain region 207' and the PWL 203 to impart a potential to the pixel electrode 213 through the aluminum electrode 209. The potential application to the gate electrode 205 is suspended when the potential of the pixel electrode 213 reaches a given value so that the pixel **switching transistor** is in an OFF state. The signal charge accumulated in the pn-junction capacitor fixes the potential of the pixel electrode 213 before the pixel **switching transistor** is redriven. The fixed potential of the pixel electrode 213 drives the liquid crystal 214 encapsulated between the substrate 201 and the counter substrate 220 shown in FIG. 32H.

Claims Text - CLTX (13):
12. A matrix substrate according to claim 1, wherein said pixels are connected to **switching transistors**.

Claims Text - CLTX (14):
13. A matrix substrate according to claim 12, wherein each of the **switching transistors comprises a CMOS** device.

Claims Text - CLTX (27):
25. A liquid crystal device according to claim 14, wherein said pixels are connected to **switching transistors**.

Claims Text - CLTX (28):
26. A liquid crystal device according to claim 25, wherein each of the **switching transistors comprises a CMOS** device.